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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional): MTKP0032USA

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on 07/09/2008

Signature Janice Chen

Typed or printed name Janice Chen

Application Number	Filed
10/604,862	08/22/2003

First Named Inventor: Ming-Yang Chao

Art Unit	Examiner
2627	Gupta, Parul H

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
- ☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- ☑ attorney or agent of record. Registration number 41,526.
- ☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

Winston Hsu
Signature

Winston Hsu
Typed or printed name

302-729-1562
Telephone number

07/09/2008
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

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HIGH-SPEED OPTICAL RECORDING APPARATUS

Appl. No.	:	10/604,862	Confirmation No.	: 1861
Applicant	:	Ming-Yang Chao		
Filed	:	August 22, 2003		
TC/A.U.	:	2627		
Examiner	:	Gupta, Parul H		
Docket No.	:	MTKP0032USA		
Customer No.	:	27765		

Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Reconsideration and allowance of claims 1, 4-14, 18, 40, and 43-47 is respectfully requested because the independent claims 1 and 40 have been rejected based on an improper standard. Specifically, the Examiner's rejection of independent claims 1 and 40, in addition to other dependent claims, does not sufficiently teach all of the limitations of the claims. According to MPEP 2143.03 "All words in a claim must be considered in judging the patentability of that claim against the prior art".

Concerning independent claim 1:

Claim 1 recites that a clock generator generates distinct first and second clock signals. Claim 1 also states that a delay adjustment state machine generates a rough delay parameter and a fine delay parameter according to the selected set of write strategy parameters, and delays the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal.

In contrast, the cited prior art fails to disclose the delay adjustment state machine

"delaying the RLL modulation waveform according to the second clock signal and the set of write strategy parameters so as to generate a second delay signal".

As evidenced by the most recent Office action dated March 10, 2008, the Examiner's position is that:

a) The delay adjustment state machine is part of element 114 (Fig. 2 of Kaku).

b) The second clock signal refers to SCLK and is transferred to the delay adjustment state machine through the "internal data bus" shown in Fig. 2 of Kaku.

c) The delay adjustment state machine delays the RLL modulation waveform according to the second clock and the set of write strategy parameters (Column 2, lines 38-40 of Kaku).

However,

a) Kaku fails to disclose that the "internal data bus" transfers the clock signal SCLK into the write strategy control unit 104. As one can see, Kaku only illustrates the internal data bus in Fig. 2, but fails to provide more detailed descriptions, such as, what the structure of the bus is and how the bus operates. Therefore, one of skilled in the art cannot realize how the "SCLK is transferred to the delay adjustment state machine through the internal data bus".

b) Further, Kaku fails to disclose the delay adjustment state machine delays the RLL modulation waveform according to the second clock and the set of write strategy parameters. The cited paragraph (col. 2, lines 38-40) only disclose "For this the delay circuit is provided for the purpose of bring the NRZ modulation signal from the modulation circuit into line with the reflection light in timing thereof". From this one skilled in the art cannot realize how the teaching of this paragraph has a relationship with "the delay adjustment state machine", and further has the relationship with the delay adjustment state machine "<u>delaying the RLL modulation waveform according to the second clock and the set of write strategy parameters</u>".

In the Response to Arguments written on page 12 of the Office action dated 03/10/2008, the Examiner has stated that "Applicant argues that Kaku et al. does not teach that the internal data bus transfers the clock signal to the write strategy control unit. However, as the data utilizes this clock (it is the only one feeding into element 100) the data bus also carries the same clock signal."

The applicant respectfully submits that the examiner is reading too much into the disclosure of Kaku, and that Kaku's disclosure does not teach or suggest how "the data utilizes the clock". Since the second clock does not enter the write strategy unit 104, the write strategy unit 104 does not have the ability to delay the RLL modulation waveform according to the second clock signal.

Therefore, the applicant submits that claim 1 is patentable over the combination of Kaku and Kato for the reasons given above. Furthermore, as claims 4-14, 18, and 43-47 are dependent on claim 4-14, 18, and 43-47 should be allowed if claim 1 is allowed.

Concerning independent claim 40:

Claim 40 recites the limitation of "wherein the fine delay chain is not connected to and does not utilize a clock signal for delaying the first delay signal to generate the write signal."

The fine delay chain is utilized to process "the first delay signal". Before the first delay signal is processed by the fine delay chain, the first delay signal might be generated associating with a clock signal. However, when the fine delay chain delays the first delay signal, it is not needed to connect and utilize a clock signal. Thus, one skilled in the art would not interpret that the fine delay chain, as shown in Figs. 2 and 3 of the instant application, delays **the first delay signal** by utilizing a clock signal.

The Examiner has stated at the end of page 12 of the Office action dated 03/10/2008, "However, by not utilizing a clock signal in the generation of the delay

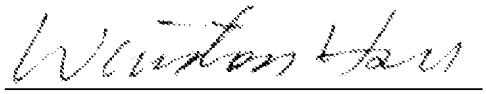
parameters, Kato et al. does not utilize a clock signal in delaying the first delay. If no clock signal was utilized in generating a delay parameter, no clock signal can be utilized while the parameter is implemented."

However, Kato teaches in column 5, lines 50-53 that the fine delay 234 "**be clocked** so as to produce a different delay". Also, Figure 3 teaches that the clock signals ($4f_{EFM\ \Phi 0\text{-}\Phi 7}$) are sent to the fine delay 324 to be used as an input for creating a delay with the fine delay 324. Therefore, for the above reasons, the applicant respectfully submits that claim 40 is patentable over the combination of Kaku and Kato.

Conclusion:

Thus, the applicant submits that all pending claims are in condition for allowance with respect to the cited art for at least the reasons presented above. A pre-appeal brief conference to review the above arguments is respectfully requested.

Sincerely yours,



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